CLAIMS

1. A computer system, comprising:

an input device;

an output device;

a data storage device;

a processor coupled to the input device, the output device and the data storage device, the processor including an address bus, a control bus and a data bus to communicate address, control and data signals;

a memory device coupled to the processor, the memory device including address, data and command busses; and

a configuration circuit interposed between at least one of the address, control and data buses of the processor and the respective address, control and data buses of the memory device to selectively couple lines in at least one of the address, control and data busses of the processor to lines in at least one of the address, control and data busses of the memory device.

2. The system of claim 1, wherein the configuration circuit comprises at least one bi-stable relay device.

3. The computer system of claim 1, wherein the configuration circuit comprises one or more Micro-Electrical-Mechanical System (MEMS) relays formed within the memory device to selectively couple lines in the address, control and data busses of the processor to lines in the address, control and data busses of the memory device.

4. The computer system of claim 1, wherein the configuration circuit is coupled to at least one of an address decoder, a command decoder and a read/write circuit in the memory device.

5. The computer system of claim 1, wherein the configuration circuit comprises an address configuration circuit interposed between the address bus of the processor and the address bus of the memory device, and further wherein the configuration circuit includes a data configuration circuit interposed between the data bus of the processor and the data bus of the memory device.

6. The computer system of claim 5, wherein the address configuration circuit and the data configuration circuit are coupled to a configuration control line.

7. The computer system of claim 1, wherein the configuration circuit comprises a control configuration circuit interposed between the control bus of the processor and the control bus of the memory device.

8. The computer system of claim 7, wherein the control configuration circuit is coupled to a configuration control line.

9. The computer system of claim 1, wherein the memory device comprises more than one memory die, and the configuration circuit is interposed between the processor and the more than one memory die to selectively couple at least one of the memory die to the processor.

10. The computer system of claim 1, wherein the memory device comprises a DRAM memory device.

11. The computer system of claim 1, wherein the memory device comprises a SRAM memory device.

12. The computer system of claim 1, wherein the memory device comprises a non-volatile memory device.

13. The computer system of claim 1, wherein the memory device comprises a flash memory device.

14. A memory device, comprising:

a memory cell array having a plurality of individually addressable memory locations, the memory cell array being coupleable to one or more signal busses of an external device; and

a configuration circuit interposed between the memory cell array and the one or more signal busses of the external device to selectively couple portions of the one or more busses to the memory cell array.

15. The memory device of claim 14, wherein the configuration circuit comprises at least one bi-stable relay device.

16. The memory device of claim 14, wherein the configuration circuit comprises one or more Micro-Electrical-Mechanical System (MEMS) relays to selectively couple portions of the one or more busses to the memory cell array.

17. The memory device of claim 16, wherein the one or more busses comprise a plurality of discrete signal lines, and further wherein the MEMS relays selectively couple the signal lines to the memory cell array.

18. The memory device of claim 14, further comprising:

an address bus coupled to the memory cell array to transfer a selected memory address location from a corresponding bus of the external device to the memory cell array;

a data bus coupled to the memory cell array to transfer data from a corresponding bus of the external device to the selected memory address location in the memory cell array;

an address configuration circuit coupled to the address bus that selectively couples one or more signal lines in the address bus to the memory cell array; and

a data configuration circuit coupled to the data bus that selectively couples one or more signal lines in the data bus to the memory cell array.

19. The memory device of claim 18, wherein the address bus further comprises an address decoder, and the data bus further includes a read/write decoder.

20. The memory device of claim 18, further comprising:

a control bus coupled to the memory cell array to transfer selected control signals from a corresponding bus of the external device to the memory cell array; and

a control configuration circuit coupled to the control bus that selectively couples one or more signal lines in the control bus to the memory cell array.

21. The memory device of claim 20, wherein the control bus further comprises a command decoder.

22. A selectively configurable memory device, comprising:

a first memory die having a first memory capacity;

a second memory die having a second memory capacity; and

a configuration circuit operable to couple either or both of the first memory die and the second memory die to external circuits to selectively obtain a memory device having a third memory capacity.

23. The selectively configurable memory device of claim 22, wherein the first memory capacity is approximately equal to the second memory capacity, and the third memory capacity is approximately equal to a sum of the first memory capacity and the second memory capacity.

24. The selectively configurable memory device of claim 22, wherein the third memory capacity is approximately equal to one of the first memory capacity and the second memory capacity.

25. The selectively configurable memory device of claim 22, wherein the configuration circuit is further coupled to a plurality of signal pins to couple signals from the external circuits to the memory device.

26. The selectively configurable memory device of claim 22, wherein the configuration circuit includes at least one bi-stable relay device.

27. The selectively configurable memory device of claim 22, wherein the configuration circuit comprises one or more Micro-Electrical-Mechanical System (MEMS) relays operable to couple either or both of the first memory die and the second memory die to the external circuits.

28. The selectively configurable memory device of claim 22, further comprising a third memory die having a fourth memory capacity.

29. A method of testing a memory device having a memory cell array, comprising:

subjecting the memory device to a first test procedure to determine the operability of the device, the memory device having a first configuration;

packaging the memory device in a device package;

configuring the memory device to have a second configuration different from the first configuration; and

after configuring the memory device to the second configuration, subjecting the packaged device to a second test procedure to verify the operability of the memory device.

30. The method of claim 29, wherein the first and second test procedures test the memory cell array of the memory device.

31. The method of claim 29, wherein the first and second test procedures are wide test procedures.

32. The method of claim 29, wherein packaging the memory device further comprises connecting the memory device to a plurality of pins coupled to a package

33. The method of claim 32, wherein the memory device includes a configuration circuit coupled to the memory array, and configuring the memory cell array further comprises applying a configuration signal to the configuration circuit to convert the memory device from the first memory configuration to the second memory configuration.

34. The method of claim 33, wherein applying a configuration signal to the configuration circuit further comprises determining a state in at least one bi-stable relay device within the configuration circuit.

35. The method of claim 33, wherein applying a configuration signal to the configuration circuit further comprises altering the position in at least one Micro-Electrical-Mechanical System (MEMS) relay within the configuration circuit.

36. The method of claim 29, further comprising establishing a desired memory configuration subsequent to the second test procedure.

37. The method of claim 29, wherein the memory device comprises a first memory capacity, and subjecting the memory device to a first test procedure further comprises

determining the operability of the memory cell array; and if the memory cell array is partially operable, reconfiguring the memory device to have a second memory capacity that is less than the first memory capacity.